Product Data Sheet

Model no: 20J6

Version 1.1

MicroJet Technology Co., Ltd.

Product Specifications

Sensor Specifications

	Type	CMOS camera module (**OV 9650** INSIDE)
	Active Array Size	1300*1028 pixels
Power Supply	**Core**	1.8VDC±10%
	Analog	2.45 to 2.8 VDC
	I/O	2.5V to3.3 DC
Power Requirements	**Active**	50mW(15 fps, no I/O power)
	Standby	30 μ W
Temperature Range	**Operation**	-20℃ to 70℃
	Stable Image	0℃ to 50℃
Output Format (8-bit)		YUV/YCbCr 4:2:2
		GRB 4:2:2
		Raw RGB Data
Maximum Image Transfer Rate	**SXGA**	15fps
	VGA	30fps
	QVGA,QQVGA,CIF	60fps
	QCIF,QQCIF	120fps
	Sensitivity	0.9V/Lux-sec
	S/N Ratio	40 dB
	Dynamic Range	62 dB
	Scan Mode	Progressive
	Maximum Exposure interval	1050 × t_{ROW}
	Gamma Correction	Programmable
	Pixel Size	3.18 μ m*3.18 μ m
	Dark Current	30mV/s at 60℃
	Well Capacity	28Ke
	Fixed Pattern Noise	<0.03% of $V_{PEAK\ TO\ PEAK}$
	Image Area	4.13mm*3.28mm
	Package Dimensions	5095 μ m*5715 μ m

Optical Specifications

Parameter	Specification
Lens Elements	3 GROUP(1G+2P)
Viewing Angle	57.50° diagonal
Focal Length	4.85 mm
F Number	2.8
IR-CUT Coating	IR cut Included (650+/-10nm)
TV Distortion	Under 1.0%
Effective photography distance	30cm~infinity

Pin description

Pin Location	Name	Pin Type	Function/Description
A1	PWDN	Function (default= 0)	Power Down Mode Selection-active high, internal pull-down resister 0: Normal mode 1: Power down mode
A2	AVDD	Power	Analog power supply(V_{DD-A} =2.45 to 2.8 VDC)
A3	SIO_D	I/O	SCCB serial interface data I/O
A4	D2	Output	Output bit[2]- LSB for 8-bit YUV or RGB565/RGB555
A5	D4	Output	0utput bit[4]
B1	VREF	V_{REF}	Internal voltage reference-connect to ground through 1μF capacitor
B2	NVDD	V_{REF}	Voltage reference
B3	AGND	Power	Analog ground
B4	SIO_C	Input	SCCB serial interface clock input
B5	D3	Output	Output bit[3]
C1	D0	Output	Output bit[0] –LSB for 10-bit Raw RGB data only
C2	DVDD	Power	Power supply (V_{DD-C} =1.8 VDC±10%) for digital core logic
C4	NC	-	No connection
C5	D5	Output	Output bit[5]
D1	D1	Output	Output bit [1]-for 10-bit RGB only
D2	VSYNC	Output	Vertical sync output
D4	NC	-	No connection
D5	NC	-	No connection
E1	HREF	Output	HREF output
E2	DOVDD	Power	Digital power supply (V_{DD-IO} =2.5 to 3.3 VDC) for I/O
E3	RESET	Function (default = 0)	Clears all registers and resets them to their default values. Active high, internal pull-down resistor.
E4	D8	Output	Output bit[8]
E5	D6	Output	Output bit[6]
F1	PCLK	Output	Pixel clock output
F2	XVCLK1	Input	System clock input
F3	DOGND	Power	Digital ground
F4	D9	Output	Output bit[9]-MSB for10-bit Raw RGB data and 8-bit YUV or RGB565/RGB555
F5	D7	Output	Output bit [7]

NOTE:
D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9]MSB, D[2]LSB)
D[9:0] for 10-bit Raw RGB data (D[9]MSB, D[0]LSB)

Electrical Characteristics

Absolute Maximum Ratings

Ambient Storage Temperature		-40℃ to 95℃
Supply Voltages (with respect to Ground)	V_{DD-A}	4.5V
	V_{DD-C}	3V
	V_{DD-IO}	4.5V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD_IO}+1V
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ.	Max	Unit
V_{DD-A}	DC supply voltage – Analog	-	2.45	2.5	2.8	V
V_{DD-C}	DC supply voltage – Core	-	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	-	2.25	-	3.6	V
I_{DDA}	Active (Operating) Current	See Note [a]		20		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current	See Note [b]		10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} =2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.0V,
I_{DDA} = Σ"{I_{DD-IO}+ I_{DD-C} + I_{DD-A}}, f_{CLK} = 24MHz at 7.5 fps YUV output, no I/O loading

b. V_{DD-A} =2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.0V,
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

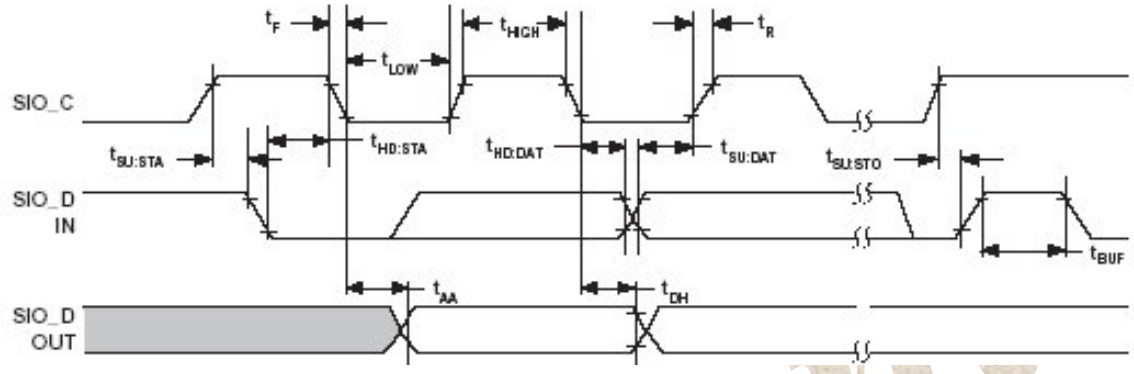
c. Standard Output Loading = 25pF, 1.2KΩ

Functional and AC Characteristics (-20°C < T_A < 70°C)

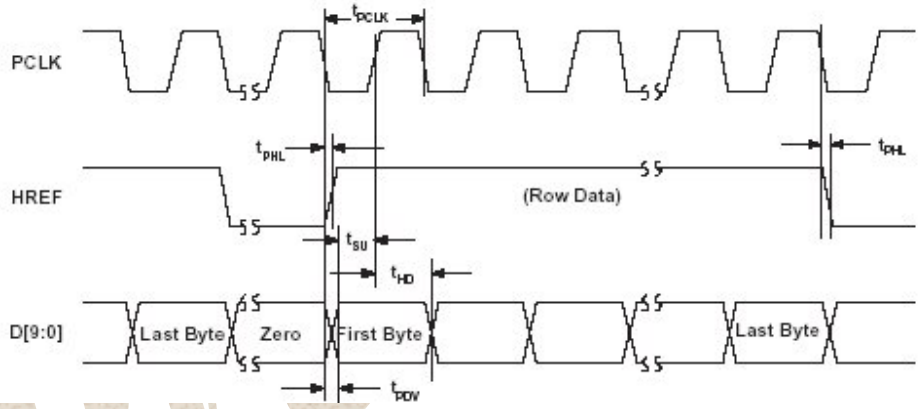
Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range		12		dB
Inputs (PWDN,CLK,RESET)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (SIO_C and SIO_D)(see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{high}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0](see Figure 5,6,7,8,9,10,11)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[9:0] Setup time	15			ns
t_{HD}	D[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions	• V_{DD}: V_{DD-C} =1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 3.0V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

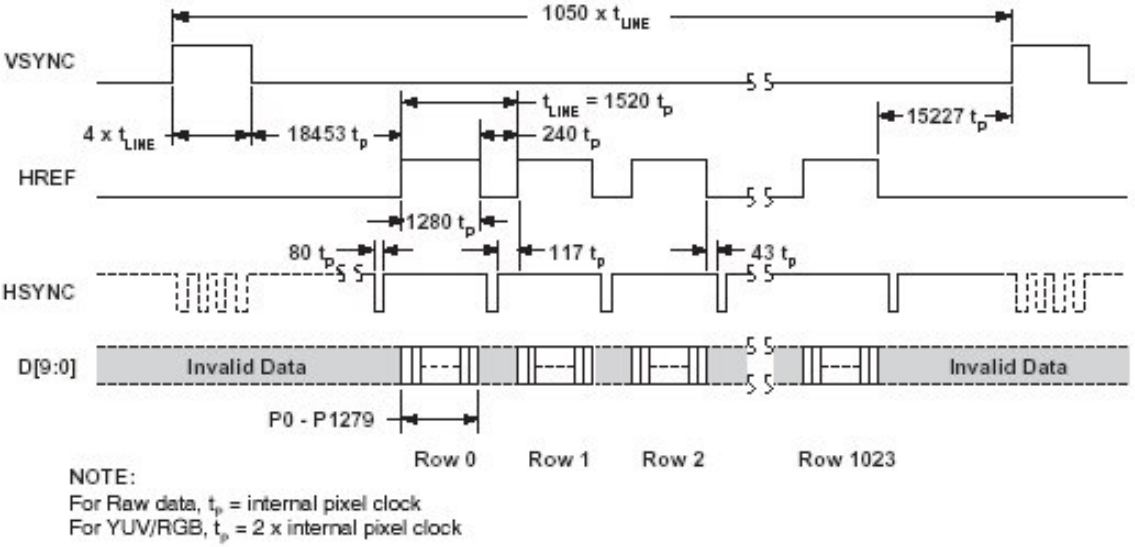
SCCB Timing Diagram



Horizontal Timing

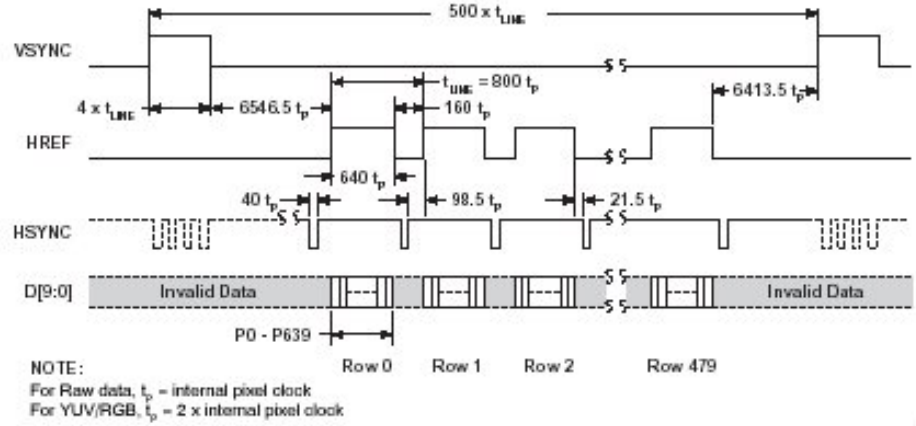


SXGA Frame Timing



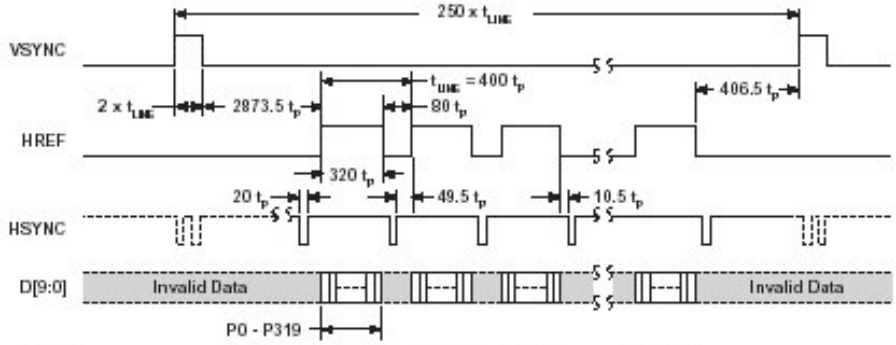
NOTE:
For Raw data, t_p = internal pixel clock
For YUV/RGB, t_p = 2 x internal pixel clock

VGA Frame Timing



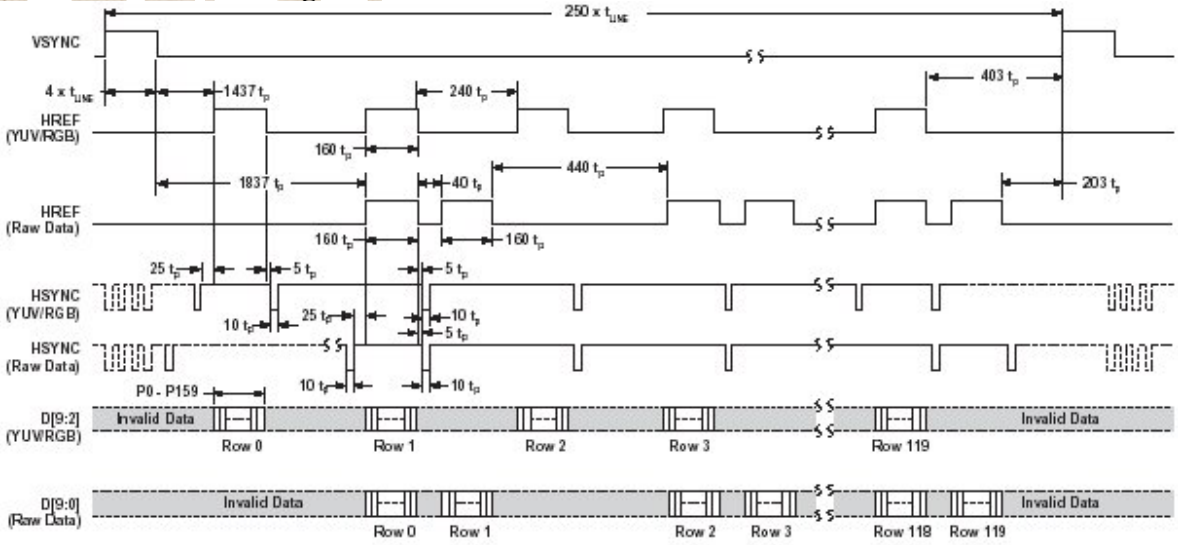
NOTE:
For Raw data, t_p = internal pixel clock
For YUV/RGB, t_p = 2 x internal pixel clock

QVGA Frame Timing



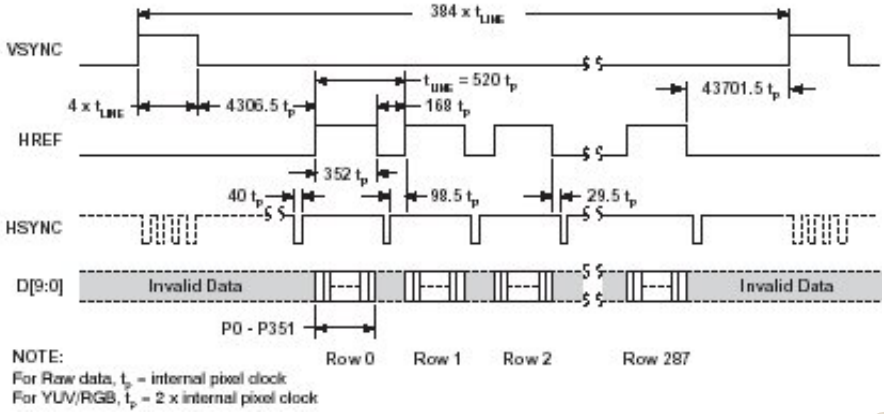
NOTE:
For Raw data, t_p = internal pixel clock
For YUV/RGB, t_p = 2 x internal pixel clock

QQVGA Frame Timing



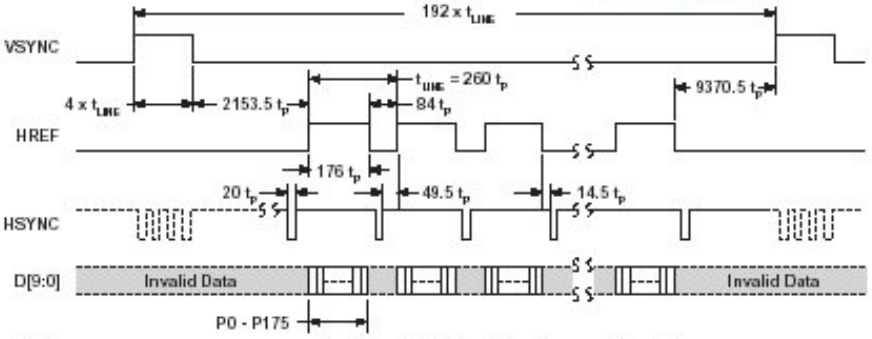
NOTE:
For YUV/RGB, t_p = 2 x t_{PCLK}
For Raw data, t_p = t_{PCLK}

CIF Frame Timing



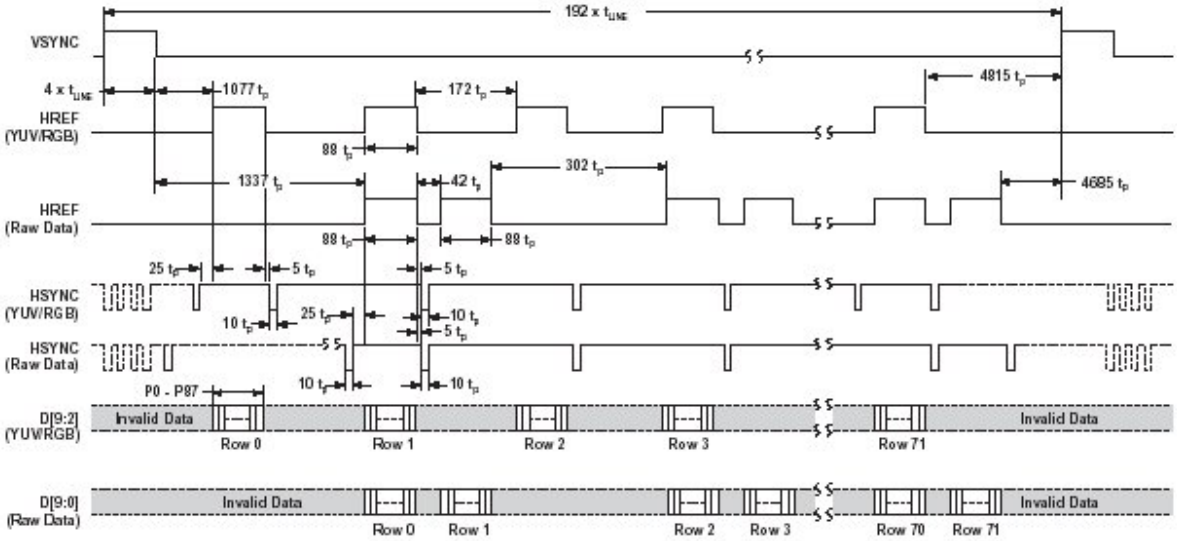
NOTE:
For Raw data, t_p = internal pixel clock
For YUV/RGB, t_p = 2 x internal pixel clock

QCIF Frame Timing



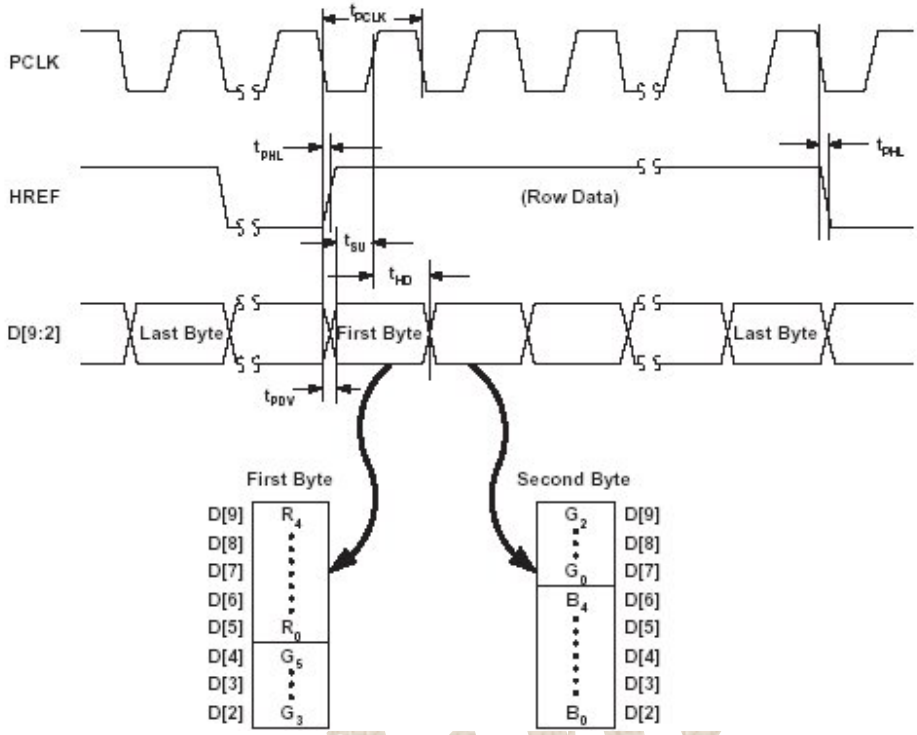
NOTE:
For Raw data, t_p = internal pixel clock
For YUV/RGB, t_p = 2 x internal pixel clock

QQCIF Frame Timing

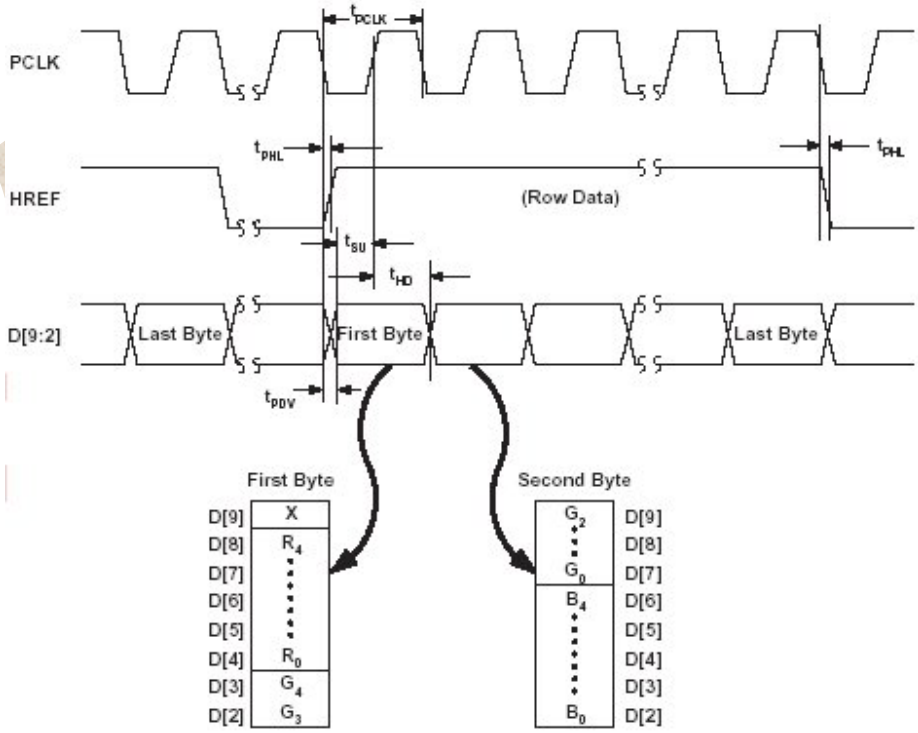


NOTE:
For YUV/RGB, t_p = 2 x t_{PCLK}
For Raw data, t_p = t_{PCLK}

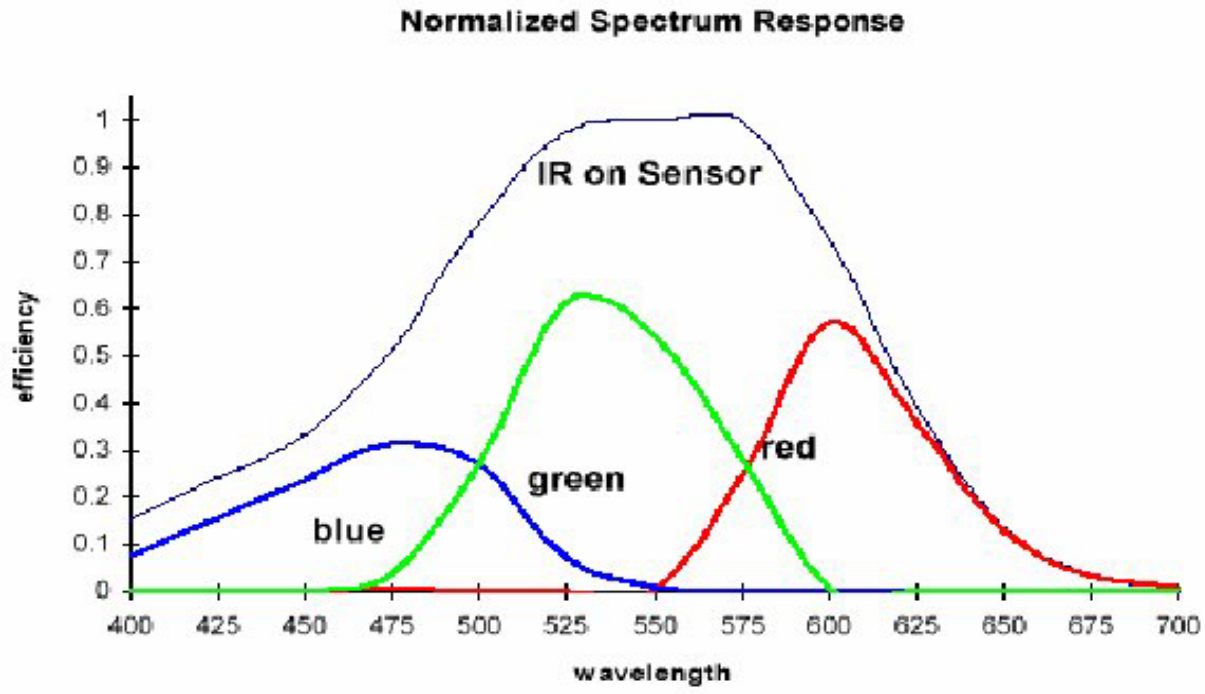
RGB 565 OUTPUT TIMING DIAGRAM



RGB 555 OUTPUT TIMING DIAGRAM



Light Response



Outline Drawing